Original Research

Optimising The Leakage Parameters Of 6T SRAM Cells Using The Laser Technique

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Abstract: In this research, we presented a technology called LECTOR that, when applied to FinFET based 6T SRAM cells, greatly reduces both static power and leakage current while having little effect on dissipated power, which is dynamic in nature. High-performance, low-leakage devices are in high demand nowadays. In order to make high-density devices with these qualities, designers are diving down to the sub-micron level. However, as a result of reducing gate oxide thickness, the overall design has resulted in an increase in sub-threshold current and, by extension, power dissipation. This work describes the 45 nm technology, Cadence Virtuoso-based design and verification of a 0.5V, 0.7V, and 1V operating voltage FinFET 6T SRAM cell using the traditional and LECTOR techniques, respectively. At 0.5 V, the leakage current is seen to drop to 39.03 fA from 66.19 fA, a reduction of 41.03%; this indicates that the approach applied in the cell may be used till 0.5 V while using 45 nm technology.

Keywords: LECTOR, 6T SRAM, power dissipation, leakage current, FinFET, CMOS.

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1 Introduction

The rising significance of portable entities and low power consuming devices to manufacture high density devices have led to increase in fast and innovative growth of devices that are small in sizes and less in leakage parameters. Another factor is the higher processing speed and superior performance at lower cost [1]. The approach towards VLSI synthesis technology has made it desirable to assemble entire system on chip (SoC) which improves the development of portable devices. Portable entities or battery operated applications for example mobile phones, computers and equipment used in military services considers power factor as a critical factor or parameter in digital domain in VLSI [2]. It is known that battery have limited life range that consistently enforces rising problem of overall power consumption of portable systems. As the scaling of technology is increasing, supply voltage (VDD) and threshold voltage (Vt) are also getting scaled down. As it is clear that these two parameters VDD and Vt of MOS transistors are critical component to maintain switching operation and performance of any cell, so it's necessary to balance all these values to have proper functioning of cell [3].

$$V_t = V_{t\text{-}mos} + V_{fb} \quad (1)$$

$$V_t = V_{fb} + \frac{\sqrt{2€q\ NA(2\Phi b+|Vsb|}}{Cox} \quad (2)$$

Due to its widespread application in System on chip and high performance VLSI circuits, SRAM's popularity continues to rise. In order to accommodate smaller, more portable battery-operated gadgets, CMOS circuits are constantly being shrunk [4]. There are a number of obstacles in the design of nanoscale CMOS SRAM memory, such as shrinking the noise margin and increasing the unpredictability. Data stored in SRAM is erased once the memory is powered. Several different chip designs with improved integration, increased speed, and decreased power consumption have been created using CMOS technology. The feature size of CMOS devices has been reduced during the last several years in order to achieve these goals. Modern microprocessors increasingly prioritise low power operation. One of the most effective methods for achieving these goals is the development of SRAM cells that need very little energy to function [5]. Memory with a higher capacity will have a higher leakage current, resulting in higher power consumption even while the device is idle. Densely packed arrays of SRAM cells are often used to build these on-chip memory cells, which allows for great performance.

New research demonstrates that standard 6T SRAM cells degrade significantly in stability while operating in low power mode as a result of access disturbance. To address the issues encountered by the 6T SRAM cell, this study proposes the construction of a 6T LECTOR (leakage Control Transistor) SRAM cell [6].

2 FinFET

Bulk CMOS and SOI CMOS not able to scaling down beyond 65nm due to the effect of short channel, leakage parameters affected mainly the sub-threshold parameters and insulation of vertical gate on wafers. The FinFET was created as a solution to MOSFET's shortcomings. Figure 1.10 describes DELTA and FinFET structure [7]. It is just a multi gate Field Effect Transistor which has been scaled further of MOSFET. It has many characteristics with a transistor, but improves upon CMOS in key ways.

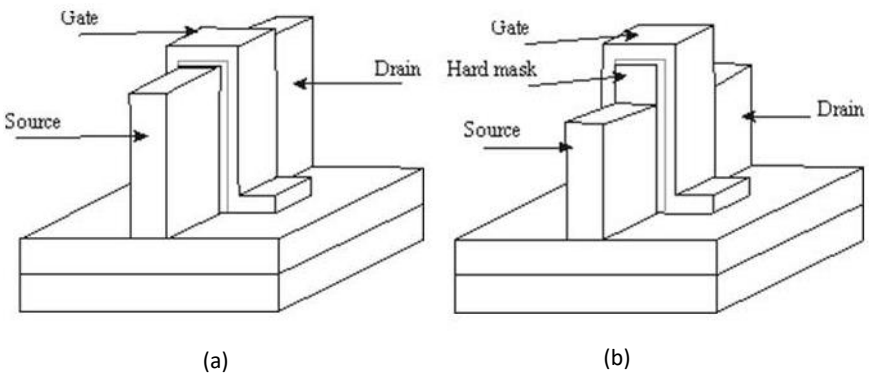

Figure 1 Double Gate MOSFET Structure: a) DELTA & b) FinFET

Double-gate FinFET device are proposed as a best and reliable replacer to the bulk CMOS scaling limit, FinFET helps to modify the device structure in such a manner so that gate length can be scaled further even with the oxide, gate width, and density of the devices on a single die, even with the less limitation over the bulk CMOS [8]. Recent work over FinFET circuits helps to reduce short channel effects but also reduces other drawbacks related to the voltage, dissipation and leakage. It also improves the speed, access time and less delay by using variable threshold voltage.

3 DOUBLE-GATE FinFET DEVICES

The enfolded gate over a very thin layer of silicon body which has thickness T_{si}, created single layer of equally doped terminals known as the FinFET device. Figure 2 shows the substrate level structure of FinFET. The structure of device helps to flow current to flow parallel to the wafer and channel is perpendicular to it [9]. That's why its name is Quasi-planar. The Effective Gate width is denoted by -

$$W_{eff} = 2nh \quad (3)$$

For a given single channel, let n be the total number of Fins and h be their average height.

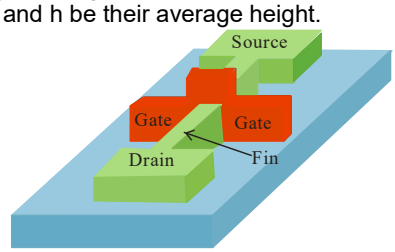

Figure 2 Substrate level structure of FinFET

Custom designers will faces that all the Fins on the same line must be the same width and height [10,11,12,13,14], they can also add and deduce the layer of Fins to control over the width of the device in fabrication process. The number of Fins in an integer form not in rational form.

4 Conventional 6T FinFET SRAM Cell

Each inverter in a 6T SRAM Cell consists of an NMOS transistor and a PMOS transistor, with an additional pair of NMOS transistors linked to the row line. A 6T Cell is the technical term for this layout. Figure 3 depicts the architecture and construction of a typical 6T SRAM cell, which is constructed using FinFETs. The bit lines BL and BLB are utilised for data reception. The WL (word line) is used for reading, whereas the BL and BLB (bit and byte lines) are used for writing.

The biggest drawback of the 6T SRAM cell is its size, and leakage characteristics appear to be significant when calculated. Up until recently, the 6T cell design was only used in industries like the military and space that required very robust immune system components. In the future, though, the 6T cell may find widespread use as businesses demand quicker SRAMs[15-16]. There are various techniques that have been discovered to overcome the leakage parameters in nanoscale regime. Every other technique faces some tradeoffs between leakage reduction, delay, power consumption etc.. FinFET technologies may be used in IoT and other semiconductor sensors as presented by different authors [17,18,19].

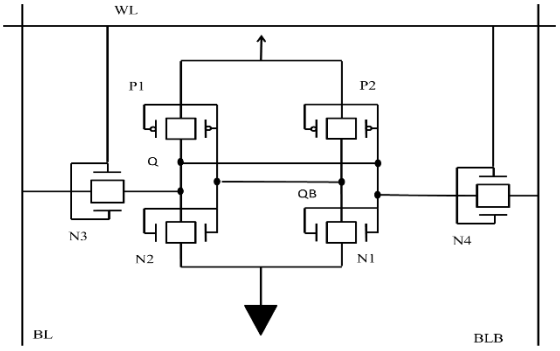

Figure 3: FinFET based 6T SRAM Cell

6 FinFET Based LECTOR Technique 6T SRAM Cell

Each CMOS transistor also makes use of the Lector method, which stands for leakage control transistor. Providing a more secure channel from VDD to ground is the primary motivation for this method. The leakage of a circuit may be reduced by using many OFF transistors in a line from VDD to ground, as opposed to using a single OFF transistor in a supply-to-ground link. The primary goal of using LCTs is to ensure that at least one LCT is always located inside or very close to the operational cutoff zone. Each leakage control transistor has its gate terminal regulated by another. This configuration helps reduce

s`ub-threshold leakage current by introducing more resistance into the route. This method is just as useful in the active state, which is an essential consideration. The lector method and lector method are shown in Figure 4. Cell SRAM 6T.

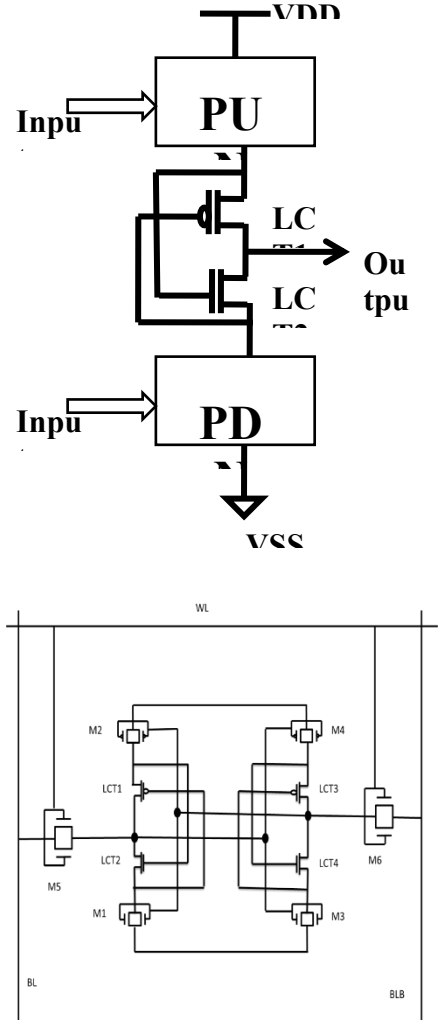

Figure 4: Lector technique block diagram and Lector 6T FinFET SRAM Cell

Similar to a standard 6T SRAM cell, the cross-coupled inverter is formed by the transistors labelled M1, M2, M3, and M4.

There are four LECTOR transistors (Leakage Control Transistors), labelled LCT1, LCT2, LCT3, and LCT4, in between. Their primary function is to be located in the route of supply to ground, close to the cut-off area that supplies the cut-off state of transistors, therefore drastically lowering leakage current.

The PULL UP and PULL DOWN circuits are separated by these leakages regulated transistors. As can be seen in the diagram, in order to maintain the necessary operation for a less leaky channel, the gate terminal of one LCT is linked to the source terminal of another.

7 SIMULATION RESULTS

Cadence Virtuoso Tool was used to simulate and verify the circuits using 45 nm technology. Equal testing circumstances have been achieved by simulating the identical input patterns into each circuit. All of these findings are from experiments conducted at ambient temperature.

The main goal of the LECTOR approach is to minimise leakage current without compromising power dissipation. When the circuit is turned off but current is still flowing, this is called sub-threshold leakage current, and it is the result of leaking. The drain current of a transistor at gate source voltages below its threshold voltage (Vs< Vth) is called sub-threshold leakage. As indicated by the equation, the drain current in the sub-threshold region is exponentially dependent on the gate-source voltage.

$I_{ds} = \alpha \exp(\frac{Vgs}{nVt})$ (4)

where Vt= KT/q which is thermal voltage whose value is 26 mV (approx.) , K is Boltzmann constant , T is the absolute temperature and q is the charge of the electron.

Generally, Gate current is the leakage current that flows when the transistor is OFF. Leakage current is the combination of sub-threshold and gate oxide leakage which is shown by the equation.

$I_{leakage}=I_{sub}+I_{gox}$ (5)

Where, I_{sub} is sub-threshold leakage current and I_{ox} is gate oxide current.

$I_{sub}=k_1We^{-\frac{Vth}{nVt}}(1-e^{-Vds/Vt})$ (6)

Where, K_1 and n are derived by the experiment, W is Gate width, Vt is thermal voltage, n is slope shape factor, Vth is threshold voltage

$I_{gox}=k_2W(\frac{V}{Tox})^2 e^{-\alpha\frac{Tox}{Vt}}$ (7)

Where, k_2 and α are derived by the experiment, T_{ox} is oxide thickness.

Table1: Simulation results of LECTOR 6T SRAM cell

VDD	6T FinFET Based SRAM Cell		FinFET Based LECTOR Technique 6T SRAM Cell	
	Leakage Current (fA)	Static Power (nW)	Leakage Current (fA)	Static Power (nW)
0.5V	66.19	40.12	39.03	27.26
0.7V	73.12	49.35	47.12	30.93
1V	80.31	51.13	53.42	39.62

Figure 5 shows leakage current waveform of conventional FinFET based 6T SRAM cell whose values at different voltages are shown in table1. Figure 9 shows leakage current of FinFET based LECTOR technique employed 6T SRAM cell. It is clear from the waveforms that in case of technique applied 6T SRAM cell spikes have been reduced to great extent.

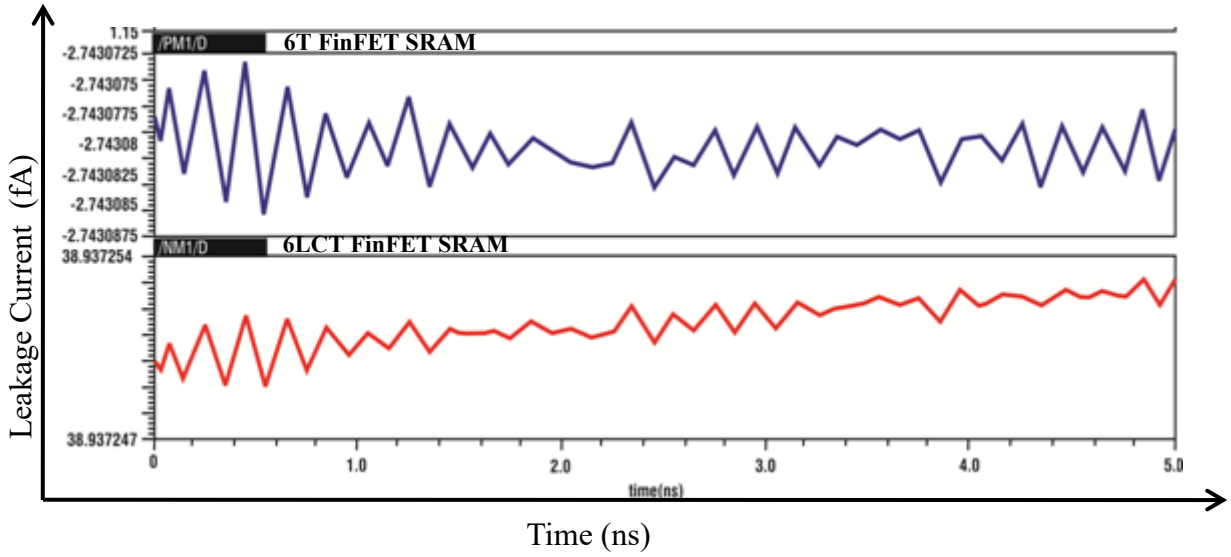

Figure 5: Leakage current of 6T FinFET SRAM and LECTOR 6T FinFET based SRAM Cell

Figure 6 represents the static power dissipation and leakage current at different supply voltages (0.3V, 0.5V and 1V) in a graphical manner that clarifies that FinFET based LECTOR 6TSRAM cell performs better than conventional FinFET 6T SRAM cell.

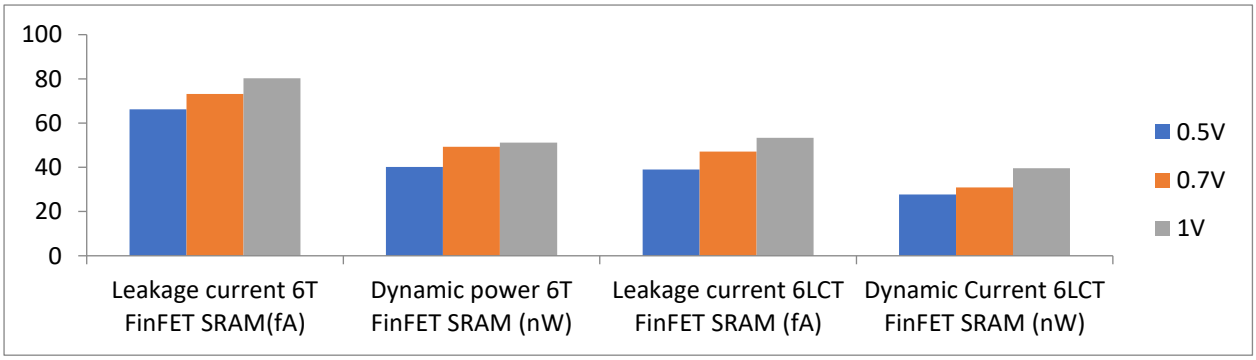

Figure 6: Graphical representation of Table 1.

10 Conclusions

Portable, convenient, wireless devices that are quick to process, operate, and have a high data density are a hot commodity in today's market. When trying to satisfy all of these criteria, traditional FinFET 6T SRAM falls short. Several leaking strategies have been developed to address these issues. Comparing standard FinFET 6T SRAM cells to those made with the LECTOR (Leakage Control Transistors) technology reveals a dramatic reduction in leakage current. About 41.03 percent of the leaking has been stopped. The equipment was able to function quickly as a consequence. This allowed for complete read/write stability in a 6T SRAM cell's operation. The cadence virtuoso tool was used to get this simulation result at 45 nm technology.

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Conflict of interest: Nil
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